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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,509	12/26/2000	Koji Hayashi	10449-030001	4131

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EXAMINER	
CHU, KIM KWOK	
ART UNIT	PAPER NUMBER
2653	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,509	HAYASHI ET AL.	
	Examiner	Art Unit	
	Kim-Kwok CHU	2653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed on 1/03/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-9* is/are rejected.

7)☒ Claim(s) *6 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless -*
> *(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.*

2. Claims 1 and 2 are rejected under 35 U.S.C. § 102(e) as being anticipated by Tsukihashi et al. (U.S. Patent 6,584,053).

Tsukihashi teaches a data buffer management device for controlling interruption and restarting of data writing to a recording medium having all the elements and means as recited in claims 1 and 2. For example, Tsukihashi teaches the following:

(a) as in claim 1, a data recording medium (Fig. 1; column 3, lines 1-6; optical head 1 is used to read/write a disk);

(b) as in claim 1, a buffer memory 12 for storing data before data written to the recording medium (Fig. 1; column 3, lines 31-34);

(c) as in claim 1, an encoder 11 connected to the buffer memory 12 (Fig. 1);

(d) as in claim 1, the encoder 11 receives data read from the buffer memory 12 (Fig. 1);

(e) as in claim 1, the encoder 11 receives data to be written to the recording medium and generates encoded data (Fig. 1);

(f) as in claim 1, a synchronizing circuit 20 for synchronizing the written data read from recording medium with the encoded data when the writing of data to the recording medium is interrupted (Fig. 1; column 3, lines 50-52; column 4, lines 5-9);

(g) as in claim 1, a first retry determination circuit 16-19 for determining whether an address of the written data, which read from the recording medium, and an address of the read data, which provided to encode, are the same (Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59);

(h) as in claim 1, a second retry determining circuit 16-19 for determining whether a timing for reading the written data from recording medium and a timing for encoding the read data are the same (Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59);

(i) as in claim 1, a restart circuit in 15 for restarting the writing of data to the recording medium based on the determining of the first and second retry determination circuits (Fig. 1; recording is resumed; column 8; lines 25-32); and

(j) as in claim 2, the second retry determination circuit determines whether the timings are the same when the first retry determination circuit determines that the addresses are the same (Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59).

3. Claims 3-5 and 7-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by Tsukihashi et al. (U.S. Patent 6,584,053).

Tsukihashi teaches a data buffer management device for controlling interruption and restarting of data writing to a recording medium having all the elements and means as recited in claims 3-5 and 7-9. For example, Tsukihashi teaches the following:

(a) as in claim 3, a data recorder medium (Fig. 1; column 3, lines 1-6; optical head 1 is used to read/write a disk);

(b) as in claim 3, a buffer memory 12 temporarily storing data before written to the recording medium (Fig. 1);

(c) as in claim 3, an encoder 11 connected to the to the buffer memory 12 (Fig. 1);

(d) as in claim 3, the encoder 11 receives data read from the buffer memory 12 and encodes the read data to generate encoded data (Fig. 1);

(e) as in claim 3, one or more address memories 15a connected to the buffer memory 12 (Fig. 1);

(f) as in claim 3, the address memories 15a store write data address of the data written to the recording medium and a read data address of the data read from the buffer memory when the writing of data to the recording medium is interrupted (Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59);

(g) as in claim 3, the write data address and the read data address each indicate a location of the data when the interruption occurs (Fig. 1; both ATIP code and sub-Q code are read and stored in address memory 15a as a starting point for continuing the recording operation; column 5, lines 38-59);

(h) as in claim 3, a synchronizing circuit 20 for synchronizing written data medium with the encoded data (Fig. 1; column 3, lines 50-52; column 4, lines 5-9);

(i) as in claim 3, a first retry determination circuit 16-19 for determining whether an address of the written data, which is read from the recording medium, and the write data address, which is stored in the one more address memories, are the same (Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59);

(j) as in claim 3, the first retry determination circuit 16-19 for determining whether an address of the read data, which is provided to the encoder from the buffer memory, and read data address, which is stored the one or more address memories, are the same (Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59);

(k) as in claim 3, a second retry determination circuit 16-19 determining whether a timing for reading the write data from the recording medium and timing for encoding the read data are the same (Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59);

(l) as in claim 3, a restart circuit in 15 restarting the writing data the recording medium based on the determinations of the first and second retry determination circuits (Fig. 1; recording is resumed; column 8; lines 25-32);

(m) as in claim 4, the written data read from the recording medium includes a first sub-code synchronizing signal and the encoded data includes a second sub-code synchronizing signal (Fig. 1; both ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59);

(n) as in claim 4, the second retry determination circuit determines whether the timing for reading the written data from the recording medium and the timing for encoding read data are the same based the first and second sub-code synchronizing signals (Fig. 1; both ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59); and

(o) as in claim 5, the second retry determination circuit determines whether the timings are the same when the first retry determination circuit determines that the addresses are the same

(Fig. 1; when recording is interrupted, ATIP code and sub-Q code are read and stored in address memory 15a; column 5, lines 38-59).

4. Claims 7-9 have limitations similar to those treated in the above rejection, and are met by the references as discussed above.

Allowable Subject Matter

5. Claims 6 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

As in claims 6 and 10, the prior art of record fails to teach or fairly suggest the following features:

(a) a first location detection circuit connected to the one or more address memories, wherein the first location detection circuit detects whether the address of the written data read from the recording and the write data address stored in the one of more address memories are the same; and

(b) a second location detection circuit connected to the one or more address memories, wherein the second location detection circuit detects whether the address of the data read from the buffer memory and the read data address stored in the one or more address memories are the same.

The features indicated above, in combination with the other elements of the claims, are not anticipated by, nor made obvious over the prior art of record.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any response to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Or faxed to:

(571) 273-8300 (for formal communications intended for entry. Or:

(571) 273-7585, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Any inquiry of a general nature or relating to the status of this application should be directed USPTO Contact Center (703) 308-4357; Electronic Business Center (703) 305-3028.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim CHU whose telephone number is (571) 272-7585 between 9:30 am to 6:00 pm, Monday to Friday.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kim-Kwok CHU
Examiner AU2653
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October 18, 2005
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